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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/816,321	03/31/2004	Jianping Xu	42P17330	9136

8791 7590 02/17/2006

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EXAMINER	
VAN ROY, TOD THOMAS	

ART UNIT	PAPER NUMBER
2828	

DATE MAILED: 02/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/816,321	XU ET AL.	
	Examiner	Art Unit	
	Tod T. Van Roy	2828	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-7,9-14,20 and 46 is/are rejected.

7)☒ Claim(s) 8,11,15 and 21 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities:

[0077] refers to a "lock recovery circuit 901", and is believed to more correctly refer to a "clock recovery circuit 901".

Appropriate correction is required.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

Claims 10 and 17 recite the limitation "the third nMOSFET" in each first line. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 4-5, 7, 9-10, 14, 16-17, and 19-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Tsai (US 6735228).

With respect to claim 1, Tsai discloses a method comprising: generating a digital voltage sequence (col.4 lines 16-17), converting the digital voltage sequence to a first current signal having an adjustable bias mode and modulation mode (via fig.3a #300, adjusted to control inputs), adjusting the bias mode of said first current signal through one or more bias control input (fig.3a #320, adjusts bias current to match control input #324), driving a first laser (fig.3a #LD302) using said first current signal to generate a first optical signal transmission.

With respect to claim 2, Tsai discloses adjusting the modulation mode of said first current signal through one or more modulation control input (fig.3a #310, adjusts bias and mod currents to match control input #314).

With respect to claim 4, Tsai discloses a method comprising: generating a digital voltage sequence (col.4 lines 16-17), converting the digital voltage sequence to a first current signal having an adjustable bias mode and modulation mode (via fig.3a #300, adjusted to control inputs), adjusting the modulation mode of said first current signal through one or more modulation control input (fig.3a #310, adjusts bias and mod currents to match control input #314), driving a first laser (fig.3a #LD302) using said first current signal to generate a first optical signal transmission.

With respect to claim 5, Tsai discloses adjusting the modulation mode of said first current signal through one or more modulation control input (fig.3a #320, adjusts bias current to match control input #324).

With respect to claim 7, Tsai discloses an optical device driver comprising: a buffered level shifter circuit to shift an input voltage to a first voltage level or to a second

voltage level (fig.3a #308, high input voltage shifted to VH1, low input voltage shifted to VL1, col.4 lines 40-44), a modulation circuit (fig.3a #306) to generate a first current signal of modulation mode responsive to the input voltage of the first voltage level (mod and bias current signal generated in #310 responsive to first voltage level VH1, fig.3a) and to generate the first current signal of a bias mode responsive to the input voltage of the second voltage level (bias current signal generated in #320 responsive to second voltage level VL1, fig.3a), a bias control circuit to adjust the bias mode of said first current signal through one or more bias control inputs (fig.3a #320 adjusts bias current to match control input #324), and a modulation control circuit to adjust the modulation mode of said first current signal through one or more modulation control inputs (fig.3a #310 adjusts bias and mod currents to match control input #314).

With respect to claim 9, Tsai discloses the modulation circuit to comprise: a pMOSFET (fig.4 above IL1 label in #430), a first nMOSFET (fig.4 below Vcc label in #420) and a second nMOSFET (Q507), the modulation circuit to cause the first current signal of the modulation mode to flow from a laser power source (Vcc in #420) through the first nMOSFET and second nMOSFET responsive to the input of the laser driver being shifted to the first voltage level (fig.3a in response to first voltage VH1), and to cause the current signal of the bias mode to flow from the laser power source through the bias control (fig.4 #430) when another current flows from a second power source (Vcc in #430) through the pMOSFET responsive to the input of the laser driver being shifted to the second voltage level (fig.3a in response to first voltage VL1).

With respect to claim 10, Tsai discloses an input gate of a third nMOSFET (fig.4 Q508) is coupled with the second power source (Vcc in #430) to reduce an overshoot of the first current signal.

With respect to claim 14, Tsai discloses an optical device driver comprising: a digital electronic interface to transmit a digital voltage input sequence (inherent in order for the sequence to be present), a buffered level shifter circuit to shift an input voltage to a first voltage level or to a second voltage level (fig.3a #308, high input voltage shifted to VH1, low input voltage shifted to VL1, col.4 lines 40-44), a modulation circuit (fig.3a #306) to generate a first current signal of modulation mode responsive to the input voltage of the first voltage level (mod and bias current signal generated in #310 responsive to first voltage level VH1, fig.3a) and to generate the first current signal of a bias mode responsive to the input voltage of the second voltage level (bias current signal generated in #320 responsive to second voltage level VL1, fig.3a), a bias control circuit to adjust the bias mode of said first current signal through one or more bias control inputs (fig.3a #320 adjusts bias current to match control input #324), and a modulation control circuit to adjust the modulation mode of said first current signal through one or more modulation control inputs (fig.3a #310 adjusts bias and mod currents to match control input #314), a laser to generate an optical signal responsive to the first current signal (fig.3a #LD302).

With respect to claim 16, Tsai discloses the modulation circuit to comprise: a pMOSFET (fig.4 above IL1 label in #430), a first nMOSFET (fig.4 below Vcc label in #420) and a second nMOSFET (Q507), the modulation circuit to cause the first current

signal of the modulation mode to flow from a laser power source (Vcc in #420) through the first nMOSFET and second nMOSFET responsive to the input of the laser driver being shifted to the first voltage level (fig.3a in response to first voltage VH1), and to cause the current signal of the bias mode to flow from the laser power source through the bias control (fig.4 #430) when another current flows from a second power source (Vcc in #430) through the pMOSFET responsive to the input of the laser driver being shifted to the second voltage level (fig.3a in response to first voltage VL1).

With respect to claim 17, Tsai discloses an input gate of a third nMOSFET (fig.4 Q508) is coupled with the second power source (Vcc in #430) to reduce an overshoot of the first current signal.

With respect to claims 19-20, Tsai discloses adjusting the modulation, and bias, modes of the current signal is accomplished by setting one or more inputs of the modulation, and bias, control (modulation and bias currents adjusted via setting of the control inputs #314, and #324 in fig.3a).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 3, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai in view of Feldman et al. (US 5978393).

With respect to claims 3, and 6, Tsai teaches the method of operating the laser driver as outlined in the rejection of claims 1 and 4 above, including use of a digital voltage input, and the adjustment of the input signal into a bias and modulation current modes. Tsai does not teach the input signal to be based on a digital clock signal, or the clock signal to be converted to a current to drive an additional laser diode. Feldman teaches a laser diode driver that uses a digital clock sequence converted to a current to drive a diode (fig.4, note digital to analog converter on clock input to circuit). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of Tsai with an additional diode laser to increase transmission capabilities of the system (well known in the art that multiple diodes can be used to provide multiple data outputs), and drive the laser with the converted clock signal of Feldman in order to reduce the amount of noise introduced into the power supply by use of the modulation current (Feldman, cols.9-10 lines 66-6).

Claims 12-13, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai in view of Bozso et al. (US 2004/0101007).

With respect to claim 12, Tsai teaches the laser driver outlined in the rejection to claim 7, but does not teach the use of CMOS circuits. Bozso teaches a VCSEL driver which uses a CMOS circuit (abs.). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the laser driver of Tsai with the CMOS circuit of Bozso in order to reduce power consumption when the logic gates are not being switched.

With respect to claims 13, and 18, Tsai teaches the laser driver outlined in the rejection to claims 7 and 14, but does not teach the laser diode to be a VCSEL. Bozso teaches a laser driver which uses a VCSEL. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the laser driver of Tsai with the VCSEL of Bozso in order to take advantage of the VCSEL's high coupling efficiency with optical fibers.

Allowable Subject Matter

Claims 8, 11, 15, and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Claims 8 and 15 are believed to be allowable as a laser driver with a buffered level shifter tunable through k+1 control signals to shift a voltage at a controlled rate with adjustable impedance responsive to a transition of a digital voltage sequence was not found to be taught in the prior art.

Claims 11 and 21 are believed to be allowable as a laser driver with a plurality of capacitors, coupled with a bias control, functioning to reduce a series resistance compared with a termination resistance was not found to be taught in the prior art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tod T. Van Roy whose telephone number is (571)272-8447. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Minsun Harvey can be reached on (571)272-1835. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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